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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/646,823

08/25/2003

Koichi Ishimi

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1807

7590

11/03/2004

McDermott, Will & Emery  
600 13th Street, N.W.  
Washington, DC 20005-3096

EXAMINER

NGUYEN, HAI L

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/646,823

Applicant(s)

ISHIMI, KOICHI

Examiner

Hai L. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 25 August 2003.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show “a first counter receiving said first initial value from said control circuit, adjusting a first count value to specify said oscillating cycle of said clock signal by using said first initial value as a first initial count value” as described in the specification (page 4, lines 23-28). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the fuse circuit (recited in claim 9) and the load circuit (recited in claim 19) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show “a counter receiving a phase comparison result and said initial value from said phase comparator and said control circuit, respectively, adjusting a count value to specify a delay amount of said first clock signal by using said initial value as a first initial count value on the basis of said phase comparison result, and outputting said adjusted count value” as described in the specification (page 5, lines 2-8). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

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even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-16 are rejected, under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed limitations that “a control circuit setting a first initial value in said clock generating circuit on the basis of a first instruction from the outside, wherein said clock generating circuit includes: a first counter receiving said first initial value from said control circuit, adjusting a first count value to specify

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said oscillating cycle of said clock signal by using said first initial value as a first initial count value”, in claim 1, have not been enabled in the specification. The details of such functions are not seen in the description of the preferred embodiment. It is not clear as currently defined, how the control circuit can perform the recited function as setting a first initial value in said clock generating circuit on the basis of a first instruction from the outside; and how the first counter can perform the recited function as adjusting a first count value to specify said oscillating cycle of said clock signal by using said first initial value as a first initial count value. Furthermore, claims 6-10 have similar problems. It is not clear as currently defined, how the detection circuit, the control circuit, the pulse counter, and the fuse circuit can perform those recited functions.

6. Claims 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed limitations that “a counter receiving a phase comparison result and said initial value from said phase comparator and said control circuit, respectively, adjusting a count value to specify a delay amount of said first clock signal by using said initial value as a first initial count value on the basis of said phase comparison result, and outputting said adjusted count value”, in claim 17, have not been enabled in the specification. The details of such functions are not seen in the description of the preferred embodiment. It is not clear as currently defined, how the counter can perform all of those recited functions. Furthermore, claim 19 has a similar problem. It is not clear as currently defined, how the load circuit can perform those recited functions.

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishimi (US pat. 6,255,840; IDS).

With regard to claim 1, Ishimi discloses in Fig. 2 an apparatus comprising a clock generating circuit generating an internal clock signal (PLL-OUT) having a frequency which is the same as or is a multiple ratio of a frequency of a reference clock signal (IN) by changing an oscillating cycle of a clock signal; and a control circuit (30) setting a first initial value in the clock generating circuit on the basis of a first instruction from the outside, wherein the clock generating circuit includes: a first counter (31) receiving the first initial value from the control circuit, adjusting a first count value to specify the oscillating cycle of the clock signal by using the first initial value as a first initial count value, and outputting the first count value (see column 12, line 64 through column 13, line 6); and an oscillation circuit (33, 34) receiving the first count value from the first counter and oscillating the clock signal on the basis of the first count value.

With regard to claims 2-4, the references also meet the recited limitations in these claims (see column 4, line 59 through column 6, line 9).

With regard to claim 5, the references also meet the recited limitations in these claims (see column 12, line 64 through column 13, line 6).

With regard to claim 17, Ishimi discloses in Fig. 2 an apparatus comprising a clock delay circuit delaying a first clock signal (PLL-OUT) to synchronize said first clock signal with a second clock signal (IN); and a control circuit (30) setting an initial value in said clock delay circuit on the basis of a first instruction from the outside, wherein said clock delay circuit

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includes: a phase comparator (35) comparing a phase of said first clock signal with a phase of said second clock signal; a counter (31) receiving a phase comparison result and said initial value from said phase comparator and said control circuit, respectively, adjusting a count value to specify a delay amount of said first clock signal by using said initial value as a first initial count value on the basis of said phase comparison result, and outputting said adjusted count value (see column 12, line 64 through column 13, line 6); and a variable delay circuit (33) receiving said count value from said counter and delaying said first clock signal on the basis of said count value.

### *Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Lane (US Pat. 5,771,264) is cited as of interest because it discloses a Digital delay lock loop for clock signal frequency multiplication circuit.


9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN   
October 27, 2004

  
TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800